Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application.

1) (previously presented) A circuit, comprising:

a clock circuit capable of generating a clock signal having a phase, the clock circuit including a phase adjuster capable of making an adjustment to the phase of the clock signal during each of a plurality of adjustment cycles in response to an adjustable phase step-size;

a sampler, coupled to the clock circuit, capable of receiving, in response to the clock signal, a data signal having a variable data bit-rate by outputting sampled data bits as received data signal; and

wherein the circuit further includes phase detection and logic circuitry capable of stalling adjustment of the phase of the clock signal during one or more current adjustment cycles in response to data phase information derived from a plurality of data bits during one or more previous adjustment cycles,

wherein the circuit further includes a phase adjust step-size logic capable of outputting the adjustable phase step-size having an adjustable magnitude dependent on the variable data bit-rate .

3) (previously presented) The circuit of claim 1, wherein the phase adjust step-size logic is capable of outputting the adjustable phase step-size having a direction dependent on the variable data bit-rate.

4) (cancelled)

5) (previously presented) The circuit of claim 1, wherein the circuit comprises 6 pipeline stages.

6) (original) The circuit of claim 1, wherein the variable data bit-rate is from approximately 0 parts per million ("ppm") to approximately 5000 ppm.

7) (original) The circuit of claim 1, wherein the adjustable phase step-size is adjusted in response to a first step-size corresponding to data phase drift and a second step-size corresponding to the variable data bit-rate.

8) (original) The circuit of claim 7, wherein the first step size and the second step-size are summed to obtain the adjustable phase step-size.

9) (cancelled)

10) (previously presented) A circuit, comprising:

a clock circuit capable of generating a clock signal in response to an adjustable phase step-size; and

a sampler, coupled to the clock circuit, capable of receiving, in response to the clock signal, a data signal having a variable data bit-rate,

wherein the circuit includes an indicator capable of adjusting the adjustable phase step-size in response to the variable data bit-rate,

wherein the circuit includes a counter for obtaining a first step-size and the indicator provides a second step-size, wherein the first step-size and the second step-size are summed to obtain the adjustable phase step-size.

11) (previously presented) The circuit of claim 10, wherein the indicator includes a state machine capable of detecting the variable data bit-rate.

12) (previously presented) The circuit of claim 1, wherein the circuit includes an averaging circuit capable of averaging a plurality of up signals to obtain an average up value and a plurality of down signals to obtain an average down value, and outputting the adjustable phase step-size in response to a comparison of the average up value and the average down value.

13) (original) The circuit of claim 1, wherein the circuit is included in a receive circuit coupled to a transmit circuit capable of transmitting the data signal.

14) (previously presented) A circuit, comprising:

a clock circuit capable of generating a clock signal in response to a phase adjust signal;

a sampler, coupled to the clock circuit, capable of receiving, in response to the clock signal, a data signal having a variable data bit-rate; and,

wherein the circuit comprises,

a first stage, coupled to the sampler, capable of outputting a first stage output signal in response to a sampled data signal;

a second stage, coupled to the first stage, capable of outputting a second stage output signal in response to the first stage output signal;

a third stage capable of outputting the phase adjust signal in response to the second stage output signal; and,

stall logic, coupled to the first, second and third stages, and capable of holding the phase adjust signal in response to the first and second stage output signals.

15) (original) The circuit of claim 14, wherein the first and second stages are successive stages.

16) (original) The circuit of claim 14, wherein the first and second stages are included in a phase detector.

17) (original) The circuit of claim 14, wherein the third stage is included in a phase adjust controller.

18) (previously presented) A circuit, comprising:

a clock circuit capable of generating a clock signal in response to a phase adjust signal having an adjustable step-size; and,

a sampler capable of receiving, in response to the clock signal, a data signal having a variable data bit-rate;

wherein the circuit includes,

a first stage, coupled to the sampler, capable of outputting a first stage output signal in response to a sampled data signal;

a second stage, coupled to the first stage, capable of outputting a second stage output signal in response to the first stage output signal;

a third stage capable of outputting the phase adjust signal, having a first step-size, in response to the second stage output signal;

stall logic, coupled to the first, second and third stages, capable of holding the phase adjust signal in response to the first and second stage output signals;

an indicator, coupled to the third stage, capable of outputting a second step-size in response to the variable data bit-rate; and,

a counter, coupled to the third stage and the indicator, capable of outputting the phase adjust signal having the adjustable step-size in response to the first and second step-sizes.

19) (original) The circuit of claim 18, wherein the first and second stages are successive stages.

20) (original) The circuit of claim 18, wherein the first and second stages are included in a phase detector.

21) (previously presented) The circuit of claim 18, wherein the counter is capable of summing the first step-size and the second step-size to provide the adjustable step-size.

22) (previously presented) The circuit of claim 18, wherein the indicator includes a state machine capable of detecting the variable data bit-rate.

23) (previously presented) The circuit of claim 22, wherein the indicator is capable of outputting a first variable frequency phase step-size in response to a first variable bit-rate in a first state and capable of outputting a second variable frequency phase step-size in response to a second variable bit-rate in a second state.

24) (original) The circuit of claim 23, wherein the first state transitions to a second state responsive to a difference of a number of up signals to a number of down signals, during a period of time, and a threshold value.

25)-29) (cancelled)

30) (previously presented) A method for tracking a signal, comprising:

receiving the signal;

outputting a plurality of digital data signals in response to an adjust signal and the signal;

selecting an update rate; and,

selecting an adjustable step-size for the adjust signal in response to the signal, wherein the selecting the adjustable step-size includes:

averaging a plurality of up signals to obtain an average up value;

averaging a plurality of down signals to obtain an average down value;

outputting the adjust signal in response to the average up value and average down value;

determining a first step-size based on a variable data bit-rate of the signal;

determining a second step-size; and

summing the first and second step-sizes to obtain the adjustable step-size.

31)-33) (cancelled)

34) (previously presented) The method of claim 30, wherein the signal is received in response to a clock signal and wherein the update rate is a divisor of a frequency of a

clock signal.

35) (previously presented) The method of claim 30, further comprising determining phase information associated with the plurality of digital data signals including:

deserializing the plurality of digital data signals to output a group of data bits in parallel;

comparing phases of the of the group of digital data bits with a phase of a clock signal to generate the plurality of up signals and the plurality of down signals; and

determining the phase information based on the plurality of up signals and the plurality of down signals.

36) (previously presented) The method of claim 30, wherein the signal is a data signal having the variable data bit-rate and the signal is received in response to the clock signal and further comprising:

updating a phase of the clock signal based on the adjustable step size.

37) (previously presented) The circuit of claim 1, wherein the circuit includes multiple pipelined stages that are controlled by a timing signal having a frequency that is a divisor of a frequency of the clock signal.

38) (previously presented) The circuit of claim 1, wherein the circuit further comprises a de-serializer coupled between an output of the sampler and the clock circuit, and wherein the circuit compares phases of a plurality of data bits output from the de-serializer with the phase of the clock signal to generate a plurality of up signals and a plurality of down signals, the circuit derives the data phase information based on the plurality of up signals and the plurality of down signals.